SPECIFICATION AMENDMENTS

Please amend the paragraph on page 1, lines 7-27 and ending on page 2, lines 1-5, as follows:

This application is related to Patent Application No. 09/232,397, filed January 15, 1999, and entitled "A METHOD FOR ROUTING INFORMATION OVER A NETWORK," having A. N. Saleh, H. M. Zadikian, Z. Baghdasarian, and V. Parsi as inventors; Patent Application No. 09/232,395, filed January 15, 1999, and entitled "A CONFIGURABLE NETWORK ROUTER," having H. M. Zadikian, A. N. Saleh, J. C. Adler, Z. Baghdasarian, and V. Parsi as inventors; Patent Application No. 09/232, ~~936~~396, filed January 15, 1999 and entitled "METHOD OF ALLOCATING BANDWIDTH IN AN OPTICAL NETWORK," having H. M. Zadikian, A. Saleh, J. C. Adler, Z. Baghdasarian, and V. Parsi as inventors; Patent Application No. 06/174,323 ~~Attorney Docket P-7241 US~~, filed ~~herewith~~ January 4, 2000, and entitled "A RESOURCE MANAGEMENT PROTOCOL FOR A CONFIGURABLE NETWORK ROUTER" having H. M. Zadikian, A. Saleh, J. C. Adler, Z. Baghdasarian and Vahid Parsi as inventors; Patent Application No. 09/477,166 ~~Attorney Docket M-7268 US~~, filed ~~herewith~~ January 4, 2000, and entitled "METHOD AND APPARATUS FOR A REARRANGEABLY NON-BLOCKING SWITCHING MATRIX," having A. N. Saleh, D. Duschatko and L. B. Quibodeaux as inventors; Patent Application No. 09/389,302, filed September 2, 1999, and entitled "NETWORK ADDRESSING SCHEME FOR REDUCING PROTOCOL OVERHEAD IN AN OPTICAL NETWORK," having A. Saleh and S. E. Plote as inventors; Patent Application No. 09/478,235 ~~Attorney Docket M-7271 US~~, filed ~~herewith~~ January 4, 2000, and entitled "A METHOD FOR PATH SELECTION IN A NETWORK," having A. Saleh as inventor; Patent Application No. 09/477,498 ~~Attorney Docket M-7272 US~~, filed ~~herewith~~ January 4, 2000, and entitled "METHOD OF PROVIDING NETWORK SERVICES," having H. M. Zadikian, S. E. Plote, J. C. Adler, D. P. Autry, and A. Saleh as inventors. These related applications are hereby incorporated by reference, in their entirety and for all purposes.

Please amend the paragraph beginning on line 1 of page 5 and ending on line 11 of page 5 as follows:

In another aspect of this embodiment, the information stream includes a number of frames. In this aspect, the error detector includes an error checker and a framing circuit. The error checker is coupled to the switching matrix and the controller, while the framing circuit is coupled to the switching matrix, the controller and the error checker. The error checker is configured to generate error check information, which is included in the error information. For example, each frame may contains an error check entry, and the error checker may generate error check information by analyzing one of the frames and comparing a result of said analyzing to an error check entry of another frame. The framing circuit is configured to detect a start-of-frame condition for each frame, indicate the start-of-frame condition to the error checker, detect an end-of-frame condition for each frame, indicate the end-of-frame condition to the error checker, and detect framing error. As with the error check information, the framing error is included in the error information.

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Please amend the paragraph beginning on line 13 of page 8 and ending on line 24 of page 8 as follows:

Fig. 1A illustrates a router 100. Router 100 includes an input/output section 110, a node controller 120, and a switching matrix 130. Node controller 120 contains, for example, real time software and intelligent routing protocols (not shown). Router wavelength 100 supports interfaces including, but not limited to, optical signal interfaces (e.g., SONET), a user interface module 150, and a management system 160. Internal input signals 170 and internal output signals 180 may be electrical or optical in nature. Fig. 1B illustrates a network 190 that includes a number of nodes, network nodes 195(1)-(N). One or more of network nodes 195(1)-(N) can be a router such as router 100. Network 190 can thus support the automatic provisioning, testing, restoration, and termination of virtual paths (exemplified by a virtual path 191) over a physical path (exemplified by a physical path 192) from one of network nodes 195(1)-(N) to another of

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network nodes 195(1)-(N). Additional physical paths 194 couple the remaining network nodes in FIG. 1B.

Please amend the paragraph beginning on line 25 of page 25 and ending on line 12 of page 26 as follows:

Assuming 16 input signals (indicated in Fig. 8 as inputs 815(1)-(16)), crosspoint switch 810 is configured to receive optical input signals from optical receivers 820(1)-(16) at switch input signals 821(1)-(16). Crosspoint switch 810 also provides switch outputs 822(1)-(17), of which switch outputs 822(1)-(16) serve as the source of output signals for switch node 800, while switch output 822(17) is used in the detection of errors. Switch output 822(17) is fed into a CDR/DEMUX 825, in which the clock is recovered and the input signal demultiplexed from a serial stream into a parallel stream. The CDR is used to re-time the serial data after the data has passed through the crosspoint switch. This helps eliminate most of the accumulated noise and jitter, and ensure that the eye opening is wide enough to carry the signal from one stage of the matrix to the next. CDR/DEMUX 825 performs two functions: first, using a stable reference clock, CDR/DEMUX 825 recovers the clock signal from the incoming data stream, then CDR/DEMUX 825 uses the recovered clock to convert the serial stream into parallel data. CDR/DEMUX 825 can also supply a 155 MHz word clock that can be used by an external physical layer processor to sample data from the device. In some embodiments, the clock and data recovery unit may include a phase-locked loop.

Please amend the paragraph beginning on line 1 of page 27 and ending on line 17 of page 27 as follows:

Fig. 9 illustrates portions of switching node 800 of Fig. 8 in greater detail. More specifically, Fig. 9 illustrates certain of the components of one embodiment of framer/error detector 830. In this embodiment, framer/error detector 830 includes an error checker 900, framing circuitry 910, an error counter 920, an error limit register 930, and a comparator 940.

Although error checker 900 and framing circuitry 910 are depicted in Fig. 9 as taking their input from CDR/demultiplexer 825, these elements could also take their input directly from crosspoint switch 810 (e.g., switch output 822(17)). Error checker 900 and framing circuitry 910 are both controlled by microcontroller 840, which downloads parameters to these elements and receives information such as error information there from. Error checker 900 and framing circuitry 910 provide error information to error counter 920, as depicted in Fig. 9. Alternatively, microcontroller 840 can interact directly with error checker 900 and framing circuitry 910 to gather and process error information directly. Error checker 900 can be one of a number of designs and perform one of several types of error analyses on the data stream being analyzed, as can framing circuitry 910. Error checker 900 can be, for example, one of a number of different types of bit parity generators. In some embodiments, error checker 900 may be configured to receive several frames in a sequence, to generate parity information for a currently-processed frame of those frames, where the currently-processed frame occurs at a particular position in the sequence, and to compare the parity information to a parity entry in another one of the frames. In one embodiment, each of the frames is a SONET frame, the parity entry is a B1 byte of a SONET frame, and the other one of the frames is at another position in the sequence that is immediately subsequent to the position in said sequence.